## AMENDMENTS IN THE CLAIMS

1. (canceled)

2. (currently amended) A self-test system for randomly adjusting the time period in which data windows are present in a data signal, comprising:

a time adjust system introducing time changes in a data window during which the data signal may be sensed; and

~~an activator~~ circuit that enables, on a random time basis, the self test system to enter into a test mode of operation, and trigger the time adjust system to introduce time delays in the data window;

wherein the time adjust system provides a delayed, test data, which is provided to an output component that accepts the delayed, test data as an output of the self test system when the self test system is in the test mode.

3. (currently amended) The self-test system of Claim 2, wherein the time adjust system introduces at least one [[of a]] time delay in an opening of the data window and an advance in a closing of the data window.

4. (canceled)

5. (currently amended) The self-test system of Claim 2, ~~wherein the activator includes~~ further comprising a random digital [[number]] sequence generator.

6. (currently amended) The self-test system of Claim 5, wherein the random digital [[number]] sequence generator comprises a linear feedback shift register.

7. (currently amended) The self-test system of Claim 5, wherein the ~~activator~~ circuit includes a decoder for detecting a presence of a defined sequence of digital code in a random digital number output of the random digital [[number]] sequence generator, wherein the defined sequence of digital code triggers an entry of the self-test system into [[a]] the test mode of operation.

8. (currently amended) The self-test system of Claim 2, wherein:

the ~~activator~~ circuit comprises:

a plurality of latches which receive even and odd alternating bits of an original sequence of incoming data bits;

a first multiplexer having inputs coupled to outputs of the plurality of latches and which recombines the incoming data bits into the original sequence; and

a decode gating circuit [[also]] coupled to the outputs of the plurality of latches and configured to identify when [[the]] a pre-set sequence of digital bits is received at the ~~activate~~ circuit; and

the time adjust system comprises a delay circuit, which receives one or more outputs from the decode gating circuit and which generates one or more delayed outputs.

9. (canceled)

10. (currently amended) A data communication system having a self-test system, said data communication system comprising:

a time adjust system introducing time changes in a data window during which data signals may be sensed; and

~~an activator~~ circuit for periodically activating, on a random basis, the self test system to enter into a test mode of operation, and trigger the time adjust system to introduce time delays in the data window;

wherein the time adjust system provides a delayed, test data, which is provided to an output component that accepts the delayed, test data as an output of the self test system when the self test system is in the test mode.

11. (currently amended) The data communication system of Claim 10, wherein the time adjust system introduces at least one [[of a]] time delay in opening the data window and an advance in closing the data window.

12. (canceled)

13. (currently amended) The data communication system of Claim 10, further comprising ~~wherein the activator includes~~ a random digital [[number]] sequence generator.

14. (canceled)

15. (currently amended) The data communication system of Claim 13, wherein the ~~activator~~ circuit includes a decoder for detecting the presence of a defined sequence of digital code in a random digital [[number]] sequence output of the random digital [[number]] sequence generator, wherein the defined sequence of digital code triggers an entry of the self-test system into [[a]] the test mode of operation.

16. (canceled)

17. (currently amended) A data communication system comprising:

a random digital sequence generator ~~("sequence generator")~~ capable of selectively issuing a series of digital 1 and 0 bits in a random sequence; and

an activate circuit coupled to an output of the sequence generator and which responds to receipt of a pre-set sequence of digital bits from the sequence generator by initiating a self-test operation by which the data communication system dynamically adjusts, on a random basis, a time period in which data windows are present within transmitting data signals, wherein the pre-set sequence indicates transmission of test data and addition of jitter to the system to perform the self-test operation.

18. (currently amended) The data communication system of Claim 17, further comprising means for introducing jitter within the data communication system and activating a self test mechanism by generating [[a]] the pre-set sequence of digital bits from the random digital sequence generator as the test data.

19. (previously presented) The data communication system of Claim 17, wherein the activate circuit comprises a time adjust system that adjusts the time period of the data windows by delaying an opening, leading edge of the data window.

20. (previously presented) The data communication system of Claim 17, wherein the activate circuit comprises a time adjust system that adjusts the time period of the data windows by advancing a closing, trailing edge of the data window.

21. (currently amended) The data communication system of Claim 17, wherein the activate circuit comprises:

a plurality of latches which receive even and odd alternating bits of an original sequence of incoming data bits;

a first multiplexer having inputs coupled to outputs of the plurality of latches and which recombines the incoming data bits into the original sequence;

a decode gating circuit [[also]] coupled to the outputs of the plurality of latches and configured to identify when the pre-set sequence of digital bits is received at the activate circuit; and

a delay circuit, which receives one or more outputs from the decode gating circuit and which generates one or more delayed outputs.

22. (currently amended) The data communication system of Claim 21, further comprising:

a time adjust system, which receives the one or more delayed outputs from the delay circuit and an output from the first multiplexer, and which adjusts selective combinations of the one or more delayed outputs and the [[said]] output from the first multiplexer by a pre-set number of delay bit periods to produce [[a]] the test [[output]] data.

23. (currently amended) The data communication system of Claim 22, further comprising:

a second multiplexer having:

a first input coupled to the output of the first multiplexer for receiving serial data transmitted through the activate circuit for normal operation;

a second input coupled to the test [[output]] data of the time adjust system for receiving test data during test operation; and

a control input at which jitter is introduced into the communication system, wherein the second multiplexer selectively outputs one of the serial data and the test data depending on the control input.

24. (previously presented) The data communication system of Claim 23, further comprising:

an optical cable drive assembly coupled to an output of the second multiplexer and which receives an output selected by the control input from the second multiplexer.

25. (previously presented) The data communication system of Claim 24, wherein:

the data communication system is a station within a fiber optic network, further comprising a fiber optic subassembly for interfacing with a fiber channel; and

the optical cable drive assembly comprises:

a first optical drive assembly providing a wrap path to a receive logic of the data communication system; and

a second optical drive assembly providing data output to the fiber channel.

26. (previously presented) The data communication system of Claim 25, wherein the random digital sequence generator comprises a linear feedback shift register.